REMARKS

As a preliminary matter, Applicants respectfully traverse the outstanding rejection in its entirety as being nonresponsive. Applicants demonstrated in Response F, filed November 22, 2006, how the Examiner has mistakenly confused switching elements and latching elements in the cited Matsueda reference (U.S. 2002/0003521) with "driving devices." All of the previous arguments are therefore incorporated by reference herein. These arguments have not been answered in the outstanding Office Action. Nowhere does the Examiner explain how switches or latches would be interpreted by one of ordinary skill in the art as a equivalent to driver, or a driving device. Accordingly, the Examiner has not satisfied his burden under Section 707.07(f) of the MPEP.

The Examiner's entire rationale for refusing to withdraw the rejection appears to be the single statement that "Applicants' BF (buffers BF) can be considered as a plurality of drivers." Whether or not this interpretation of the present Application is correct, the argument is irrelevant to the fact that Matsueda's latches and switches are not driving devices. The Examiner's focus on the buffers of the present invention has no relevance to Applicants' previous arguments because the Examiner does not even assert that Matsueda's switches or latches could alternatively be considered to be equivalent as buffers.

A "buffer" is known in the art to be an amplifier that is generally used to isolate a load from a source. A "latch," on the other hand, is known in the art as merely being the simplest form of data storage. Without some express teaching by Matsueda to the contrary, a latch would not be considered to be a driving device. A "switch" is even less likely to ever

be considered by one of ordinary skill in the art to be a driving device. A switch merely opens or closes a pathway to electric current. A switch does not drive the current through the pathway.

The repeated citation to these irrelevant elements in the Matsueda device represents a fundamental misunderstanding of the art, and therefore a clear error in the rejection. Moreover, Matsueda even teaches away from the Examiner's reliance on of the cited latching and switch elements. Matsueda expressly states in paragraph [0132] that the individual latching elements 211-216 "are respectively *driven by* the output pulses of a shift register 7." (Emphasis added). In other words, Matsueda clearly teaches that the latching elements cited by the Examiner are not drivers themselves, because they are in fact driven by another element of the unit driving circuit, namely, the shift register 7. Matsueda further clearly shows that the shift register 7 is the only "driving device" applied to an individual data line in the circuit. The reliance on the reference is thus further flawed.

With respect to the cited switches in particular from Matsueda, the Examiner appears to have concluded that switches are equivalent to buffers merely from the fact that switches are used *in cooperation with* buffers in the present invention. The fact that two separate elements may be utilized together though, hardly renders two such elements automatically equivalent to one another. As explained previously and above, switches are not drivers. Switches are passive elements with respect to a signal that passes through one of a switches pathways (or not). The switch either allows or blocks a signal, but would not be considered by one of ordinary skill in the art to affirmatively drive the signal.

The Examiner must either submit objective evidence on the record that proves how one of ordinary skill in the art would interpret a switch or a latch to be a "driving device," or the Examiner must withdrawn the outstanding rejections based in whole, or in part, on Matsueda. Such evidence would also have to clearly refute the teachings of the present Specification as well, which clearly shows switches as being separate and distinct elements from the drivers.

Claim 1 thus again stands rejected under 35 U.S.C. 102(e) as being anticipated by Matsueda. Applicants therefore respectfully traverse this rejection again for at least the reasons of record, and those discussed above. Matsueda simply does not read upon the present invention. The cited switches and latching elements from Matsueda are not driving devices, and the Examiner has submitted no evidence on the record that one of ordinary skill in the art would ever interpret such elements as reading upon the driving devices recited in the present claims.

In fact, one of ordinary skill in the art would clearly interpret the Matsueda reference to understand that all of the individual elements 211-216, 271-276, 321-325, and 341-345 each correspond to *individual respective bit signals* for expression of grayscale levels. In other words, the elements that the Examiner incorrectly asserts to be buffers actually correspond to different, single grayscale bits of the digital image signals. Accordingly, Matsueda cannot read upon the present invention for these reasons as well.

The present invention clearly features, among other things, that each data signal line is driven by a plurality of driving devices used together simultaneously. Each single data

signal of the present invention is therefore driven by a plurality of driving devices. This configuration is significantly different from Matsueda. Each of the individual elements incorrectly cited by the Examiner from Matsueda can only drive a single data signal, whereas in the present invention, a plurality of driving devices will drive each data signal. The claimed switch signals in the present invention, on the other hand, serve to control the number of the driving devices used to drive each data line. Nothing that the Examiner has cited from Matsueda even remotely reads upon this configuration. Accordingly, for at least these reasons, and/or any of the reasons discussed above, the outstanding anticipation rejection based on Matsueda should be withdrawn.

Claim 4 of the present invention again stands rejected under 35 U.S.C. 103(a) as being unpatentable over Matsueda in view of Ichikawa (U.S. 5,028,916). Applicants therefore traverse this rejection as well for at least the reasons of record and those discussed above. Ichikawa is cited merely for teaching to provide an interconnection pattern directly on a display unit instead of a separate special substrate. The Examiner does not assert that Ichikawa in any way teaches to increase the number of driving devices to an individual data line, or that Ichikawa in any way resolves these clear deficiencies from the Matsueda reference. Accordingly, this rejection should be withdrawn as well.

For all of the foregoing reasons, Applicants submit that this Application, including claims 1 and 4, is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

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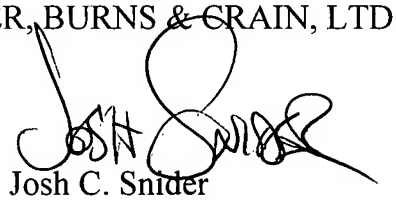
By 

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